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EXAMINER	
SAVLA, ARPAN P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/713,733	ELNOZAHY ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Appeal Brief

In view of the Appeal Brief filed on March 5, 2008, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing at the end of this action.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 7, 9-11, 14, 17, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's "Description of the Related Art", hereafter "Applicant's admitted prior art (AAPA)" in view of Armangau (U.S. Patent 6,434,681).

3. **As per claim 1**, AAPA discloses a method of assigning virtual memory to physical memory in a data processing system, comprising the steps of:

allocating a set of physical memory pages of the data processing system for a new virtual superpage mapping (pg. 5, lines 13-16);

instructing a memory controller of the data processing system to move a plurality of virtual memory pages corresponding to an old page mapping to the set of physical memory pages corresponding to the new virtual superpage mapping (pg. 5, lines 16-17). *It should be noted that the "processor" is analogous to the "memory controller."*

AAPA does not expressly disclose accessing at least one of the virtual memory pages using the new virtual superpage mapping while the memory controller is copying old physical memory pages to new physical memory pages.

Armangau discloses accessing at least one of the virtual memory pages using the new virtual page mapping while the memory controller is copying old physical memory pages to new physical memory pages (col. 2, lines 16-18; col. 15, line 52 – col. 16, line 13; Fig. 7B, elements 124-129). *It should be noted that the "snapshot volume" is analogous to the "new virtual page mapping", the "production volume" is analogous to the "old physical memory pages", and the read/write access during snapshot maintenance is analogous to access operations while copying.*

AAPA and Armangau are analogous art because they are from the same field of endeavor, that being memory mapping systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement the mapping of Armangau's snapshot volume as AAPA's superpage mapping.

The motivation for doing so would have been to reduce delay when host write access to storage locations containing original data is delayed until the original data are transmitted to a backup storage device by providing a snapshot facility in the data storage system (Armangau, col. 2, lines 4-9).

Therefore, it would have been obvious to combine AAPA and Armangau for the benefit of obtaining the invention as specified in claim 1.

4. **As per claim 2**, the combination of AAPA/Armangau discloses said allocating step allocates a contiguous set of physical memory pages (AAPA, pg. 5, lines 14-16).

5. **As per claim 3**, the combination of AAPA/Armangau discloses said accessing step includes the step of directing a read operation for an address of the new page mapping which is currently being copied to a corresponding address of an old page mapping (Armangau, col. 2, lines 16-18).

6. **As per claim 4**, the combination of AAPA/Armangau discloses said accessing step includes the step of directing a write operation for an address of the new page mapping which is currently being copied to both the address of the new page mapping and a corresponding address of an old page mapping (Armangau, col. 15, line 52 – col. 16, line 13; Fig. 7B, elements 124-129).

7. **As per claim 5**, the combination of AAPA/Armangau discloses said accessing step includes the step of directing a write operation for an address of the new page mapping which has not yet been copied to a corresponding address of an old page mapping (Armangau, col. 15, lines 43-51; Fig. 7B, elements 122 and 123).

8. **As per claim 7**, AAPA discloses a memory controller comprising:

an input for receiving remapping instructions for a virtual superpage (pg. 5, lines 16-17).

AAPA does not expressly disclose a mapping table which temporarily stores entries of old page addresses and corresponding new page addresses associated with the page remapping instructions;

and a memory access device which directs the copying of memory pages from the old page addresses to the new page addresses while handling access operations which use the new page addressees, and releases the entries in said mapping table as copying for each entry is completed.

Armangau discloses a mapping table which temporarily stores entries of old page addresses and corresponding new page addresses associated with the page remapping instructions (col. 6, lines 42-48; Fig. 1, elements 20, 21, and 24); *It should be noted that the "backup command" is analogous to "remapping instructions."*

and a memory access device which directs the copying of memory pages from the old page addresses to the new page addresses while handling access operations which use the new page addressees, and releases the entries in said mapping table as copying for each entry is completed (col. 2, lines 16-18; col. 15, line 52 – col. 16, line

13; Fig. 7B, elements 124-129; col. 6, lines 42-50; col. 7, line 65 – col. 8, line 3; Fig. 1, element 21; Fig. 3, element 51). *It should be noted that the "storage controller" within the "primary data storage subsystem" is analogous to the "memory access device."*

AAPA and Armangau are analogous art because they are from the same field of endeavor, that being memory mapping systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement the mapping of Armangau's snapshot volume as AAPA's superpage mapping.

The motivation for doing so would have been to reduce delay when host write access to storage locations containing original data is delayed until the original data are transmitted to a backup storage device by providing a snapshot facility in the data storage system (Armangau, col. 2, lines 4-9).

Therefore, it would have been obvious to combine AAPA and Armangau for the benefit of obtaining the invention as specified in claim 7.

9. **As per claim 9**, the combination of AAPA/Armangau discloses said memory access device directs a read operation for a new page address which is currently being copied to a corresponding old page address (Armangau, col. 2, lines 16-18).

10. **As per claim 10**, the combination of AAPA/Armangau discloses said memory access device directs a write operation for a new page address which is currently being copied to both the new page address and a corresponding old page address (Armangau, col. 15, line 52 – col. 16, line 13; Fig. 7B, elements 124-129).

11. **As per claim 11**, the combination of AAPA/Armangau discloses said memory access device directs a write operation for a new page address which has not yet been copied to a corresponding old page address (Armangau, col. 15, lines 43-51; Fig. 7B, elements 122 and 123).

12. **As per claim 14**, AAPA discloses a computer system comprising:

a new virtual superpage mapping (pg. 5, lines 13-16).

AAPA does not expressly disclose a processing unit;

an interconnect bus connected to said processing unit;

a memory array;

and a memory controller connected to said interconnect bus and said memory array, wherein said memory controller copies memory pages from old page addresses to new page addresses according to a new virtual superpage mapping while handling access operations which use the new page addresses and while said processing unit carries out program instructions using the new page addresses.

Armangau discloses a processing unit (col. 6, lines 1-2; Fig. 1, element 20);

an interconnect bus connected to said processing unit (Fig. 1, the "line" (i.e. bus) between the host the primary data storage subsystem)

a memory array (col. 6, lines 3-6; Fig. 1, element 27);

and a memory controller connected to said interconnect bus and said memory array, wherein said memory controller copies memory pages from old page addresses to new page addresses according to a new virtual superpage mapping while handling access operations which use the new page addresses and while said processing unit

carries out program instructions using the new page addresses (col. 2, lines 16-18; col. 15, line 52 – col. 16, line 13; Fig. 7B, elements 124-129; col. 6, lines 42-50; Fig. 1, element 21; Fig. 3, element 51). *It should be noted that the "storage controller" within the "primary storage subsystem" is analogous to the "memory controller."*

AAPA and Armangau are analogous art because they are from the same field of endeavor, that being memory mapping systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement the mapping of Armangau's snapshot volume as AAPA's superpage mapping.

The motivation for doing so would have been to reduce delay when host write access to storage locations containing original data is delayed until the original data are transmitted to a backup storage device by providing a snapshot facility in the data storage system (Armangau, col. 2, lines 4-9).

Therefore, it would have been obvious to combine AAPA and Armangau for the benefit of obtaining the invention as specified in claim 14.

13. **As per claim 17**, the combination of AAPA/Armangau discloses said cache modifies the address tag of the cache entry in response to a determination that the cache entry contains a valid value which is not present elsewhere in the system (Armangau, col. 10, lines 50-67).

14. **As per claim 19**, the combination of AAPA/Armangau discloses said memory controller includes:

a mapping table which temporarily stores entries of old page addresses and corresponding new page addresses (Armangau, col. 7, lines 18-20; Fig. 1, element 26); *See the citation note for the similar limitation in claim 7 above.*

and a memory access device which directs the copying of the memory pages from the old page addresses to the new page addresses and releases the entries in said mapping table as copying for each entry is completed (Armangau, col. 6, lines 42-50; col. 7, line 65 – col. 8, line 3; Fig. 1, element 21). *See the citation note for the similar limitation in claim 7 above.*

15. **As per claim 20**, the combination of AAPA/Armangau discloses said processing unit, said interconnect bus, said memory array and said memory controller are all part of a first processing cluster, and further comprising a network interface which allows said first processing cluster to communicate with a second processing cluster, said memory controller having at least one pointer for a new page address which maps to a physical memory location in said second processing cluster (Armangau, col. 6, lines 1-3; Fig. 1, element 22). *It should be noted that the "second storage subsystem" is analogous to the "second processing cluster." It should also be noted that it is inherently required the second storage subsystem include some sort of "interface" in order to communicate with the first storage subsystem.*

16. Claims 6 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Armangau as applied to claims 1 and 14 above, and further in view of Christie (U.S. Patent 6,175,906).

17. **As per claim 6**, the combination of AAPA/Armangau discloses all the limitations of claim 6 except the step of updating an entry in a cache memory of the data processing system which corresponds to a memory location in the virtual memory page, by modifying an address tag of the cache entry according to the new page mapping.

Christie discloses the step of updating an entry in a cache memory of the data processing system which corresponds to a memory location in the virtual memory page, by modifying an address tag of the cache entry according to the new page mapping (col. 4, lines 40-50). *It should be noted that "invalidating" the tags is analogous to "modifying" the tags.*

The combination of AAPA/Armangau and Christie are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Christie's revalidation of virtual tags within AAPA/Armangau's storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of increasing speed of recovery from remapping by reducing the number of TLB accesses during virtual-to-physical memory remapping.

Therefore, it would have been obvious to combine AAPA/Armangau and Christie for the benefit of obtaining the invention as specified in claim 6.

18. **As per claim 16**, the combination of AAPA/Armangau/Christie discloses said processing unit has a processor core and an associated cache (Armangau, Fig. 1, element 21; Fig. 3, element 52);

and said cache modifies an address tag of a cache entry which corresponds to a memory location in the new page addresses (Christie, col. 4, lines 40-50).

19. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Armangau as applied to claim 7 above, and further in view of Romer et al. "Reducing TLB and Memory Overhead Using Online Superpage Promotion", (hereinafter "Romer").

20. **As per claim 8**, the combination of AAPA/Armangau discloses all the limitations of claim 8 except said mapping table has 32 slots for receiving corresponding pairs of the old page addresses and new page addresses.

Romer discloses said mapping table has 32 slots for receiving corresponding pairs of the old page addresses and new page addresses (pg. 178, italicized section entitled "Table 2", line 4). *It should be noted that the "entries" is analogous to the "slots."*

The combination of AAPA/Armangau and Romer are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Romer's 32 slot TLB as AAPA/Armangau's primary directory.

The motivation for doing so would have been to improve system performance by increasing instructions per TLB miss (Romer, pg. 187, section entitled "Capacity Counters", last paragraph).

Therefore, it would have been obvious to combine AAPA/Armangau and Romer for the benefit of obtaining the invention as specified in claim 8.

21. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Armangau as applied to claim 7 above, and further in view of Waldspurger et al. (U.S. Patent 6,725,289) (hereinafter "Waldspurger").

22. As per claim 12, thr combination of AAPA/Armangau discloses all the limitations of claim 12 except said memory access device includes a state engine which sequentially reads the paired old and new pages addresses in said mapping table.

Waldspurger discloses said memory access device includes a state engine which sequentially reads the paired old and new pages addresses in said mapping table (col. 7, lines 26-36; col. 11, lines 13-21 and 52-62; Fig. 2, element 610). *It should be noted that the "mapping module" is analogous to the "state engine" and that "page numbers" are analogous to "page addresses." It should also be noted that the mapping module reads both the old page numbers and new page numbers because it reads the page numbers before the remapping (i.e. the old or original page numbers) and also reads the page numbers after remapping (i.e. the new page numbers).*

The combination of AAPA/Armangau and Waldspurger are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Waldspurger's transparent address remapping within AAPA/Armangau's storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the predictable results of remapping non-contiguous pages to contiguous pages, thus avoiding the need for page splits on future transfers which will improve performance accordingly.

Therefore, it would have been obvious to combine AAPA/Armangau and Waldspurger for the benefit of obtaining the invention as specified in claim 12.

23. **As per claim 13**, the combination of AAPA/Armangau/Waldspurger discloses said memory access device further includes a direct memory access (DMA) engine controlled by said state engine which carries out actual copying of the memory pages (Waldspurger, col. 7, line 67 – col. 8, line 3; col. 8, lines 20-26; Fig. 2, element 116). *It should be noted that the "memory management unit (MMU)" is analogous to the "DMA engine."*

24. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Armangau as applied to claim 14 above, and further in view of Talluri et al. "Surpassing the TLB Performance of Superpages with Less Operating System Support" (hereinafter "Talluri").

25. **As per claim 15**, the combination of AAPA/Armangau discloses copying of memory pages by a memory controller (Armangau, col. 2, lines 16-18; col. 15, line 52 –

col. 16, line 13; Fig. 7B, elements 124-129; col. 6, lines 42-50; Fig. 1, element 21; Fig. 3, element 51).

The combination of AAPA/Armangau does not disclose said processing unit includes a processor core having a translation lookaside buffer (TLB) whose entries keep track of current virtual-to-physical memory address assignments;

and said TLB entries are updated for the new page addresses prior to completion of copying of the memory pages by the memory.

Talluri discloses said processing unit includes a processor core having a translation lookaside buffer (TLB) whose entries keep track of current virtual-to-physical memory address assignments (pg. 1, right column, first full paragraph);

and said TLB entries are updated for the new page addresses prior to completion of copying of the memory pages by the memory (pg. 3, right column, second full paragraph). *It should be noted that a "page promotion" involves copying of memory pages.*

The combination of AAPA/Armangau and Talluri are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Talluri's subblock TLB within AAPA/Armangau's storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded the

predictable results of increasing system speed by improving performance of TLBs in a superpage environment.

Therefore, it would have been obvious to combine AAPA/Armangau and Talluri for the benefit of obtaining the invention as specified in claim 15.

26. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Armangau as applied to claim 16 above, and further in view of Arimilli et al. (U.S. Patent 5,974,507) (hereinafter "Arimilli").

27. **As per claim 18**, the combination of AAPA/Armangau discloses all the limitations of claim 18 except said cache further relocates the cache entry based on a changed congruence class for the modified address tag.

Arimilli discloses said cache further relocates the cache entry based on a changed congruence class for the modified address tag (col. 6, lines 43-66). *It should be noted that the intermittent or real-time adjustment of the members (i.e. cache entries) of the congruency class is based on the modification of address bits of the cache entries.*

The combination of AAPA/Armangau and Arimilli are analogous art because they are from the same field of endeavor, that being memory systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Arimilli's programmable congruence class caching mechanism within AAPA/Armangau's storage system because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the

combination would have yielded the predictable results of improving cache efficiency by lessening eviction rates.

Therefore, it would have been obvious to combine AAPA/Armangau and Arimilli for the benefit of obtaining the invention as specified in claim 18.

Response to Arguments

28. Applicant's arguments filed July 17, 2007 with respect to **claims 1-5, 7-11, 14, 17, 19, and 20** have been fully considered but they are not persuasive.

29. With respect to Applicant's argument beginning in the last paragraph on page 5 through in the first full paragraph on page 6 of the communication filed March 5, 2008, the Examiner respectfully disagrees. Firstly, the Examiner submits that the terms processor and memory controller are terms used interchangeably within the art. In many modern CPU designs, the memory controller is in fact located on the processor die itself. Applicant has even admitted that a processor is involved with access to memory systems (see the second full paragraph on page 2 of the communication filed July 17, 2007). Notwithstanding, when looking at claims themselves, Applicant's "memory controller" merely moves (i.e. copies) memory pages corresponding to an old (i.e. original) page mapping to a new superpage mapping. AAPA's "processor" copies memory pages from an original mapping to a new superpage mapping (see Applicant's specification, pg. 5, lines 16-17).

To further the Examiner's position, the Examiner offers John L. Hennessy and David A. Patterson, Computer Organization and Design, The Hardware/Software

Interface, Second Edition (hereinafter "Patterson"), pages 657, 658, and 668 as extrinsic evidence. As can be clearly seen from Figures 8.7, 8.8, and 8.12, it is in fact the processor that manages the memory array and it is the processor that executes memory data reads and memory data writes (emphasis added). Thus, AAPA's processor provides equivalent functionality as Applicant's memory controller, as simply and broadly claimed, and therefore AAPA's processor anticipates Applicant's memory controller.

30. With respect to Applicant's argument beginning in the last paragraph on page 6 through the first full paragraph on page 7 of the communication filed March 5, 2008, the Examiner respectfully disagrees. Firstly, it is noted that the features upon which applicant relies (i.e., "hardware") are not recited in the rejected claims. The only place "hardware" is mentioned is in the title of the invention. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Secondly, even if "hardware" were recited in the claims it is well known in the art that hardware and software are logically equivalent. The Examiner has provided an excerpt from Andrew S. Tanenbaum, Structured Computer Organization, 2nd Edition, as extrinsic evidence which shows that hardware and software are logically equivalent.

31. With respect to Applicant's argument beginning in last paragraph on page 7 through the first partial paragraph on page 8 of the communication filed March 5, 2008, the Examiner respectfully disagrees. This assertion has been previously addresses by the Examiner in the Office action dated April 14, 2007 which is hereby incorporated.

The Examiner would also like to add that Applicant's argue that their "new page mapping" involves "coalescing" and that the new superpage is "different" and "more efficient", however, these features are not recited in the rejected claims. Again, although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. Thus, based on the claim language as it stands there is no change in "efficiency" between the old page mapping and the new page mapping as Applicant alleges. Also, the Examiner notes that Applicant is attacking the references individually. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). The combination of AAPA/Armangau does in fact disclose a virtual superpage mapping which is "new" because the snapshot mapping is not the exact same as the original (i.e. old) production volume due to write operations completed during the copying process. Accordingly, when taking the broadest reasonable interpretation of the limitation "new virtual superpage mapping", the combination of AAPA/Armangau sufficiently disclose said limitation.

32. With respect to Applicant's argument in the first full paragraph on page 8 of the communication filed March 5, 2008, the Examiner respectfully disagrees. Col. 15, line 52 – col. 16, line 13, Fig. 7B, elements 124-129 of Armangau clearly show that during the copying process, when a write is directed to the snapshot volume, the track is written to both the snapshot volume as well as the production volume. Accordingly, the

snapshot volume (i.e. new mapping) is accessed while the copying of data from the production volume to the snapshot volume is taking place.

33. With respect to Applicant's argument dealing with claims 3 and 9, the Examiner respectfully disagrees. Col. 15, line 52 – col. 16, line 13; Fig. 7B, elements 124-129 of Armangau clearly show that during the copying process, when a write is directed to the snapshot volume, the track is written to both the snapshot volume as well as the production volume. Accordingly, the snapshot volume (i.e. new mapping) is accessed while the copying of data from the production volume to the snapshot volume is taking place.

34. Applicant's arguments with respect to **claims 6, 12, 13, 15, 16, and 18** have been considered but are moot in view of the new grounds of rejection above.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-20** have received a first action on the merits and are subject of a first action final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571)272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
June 9, 2008

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185